Exhibit 18

JEDEC STANDARD

DDR4 Data Buffer Definition (DDR4DB02)

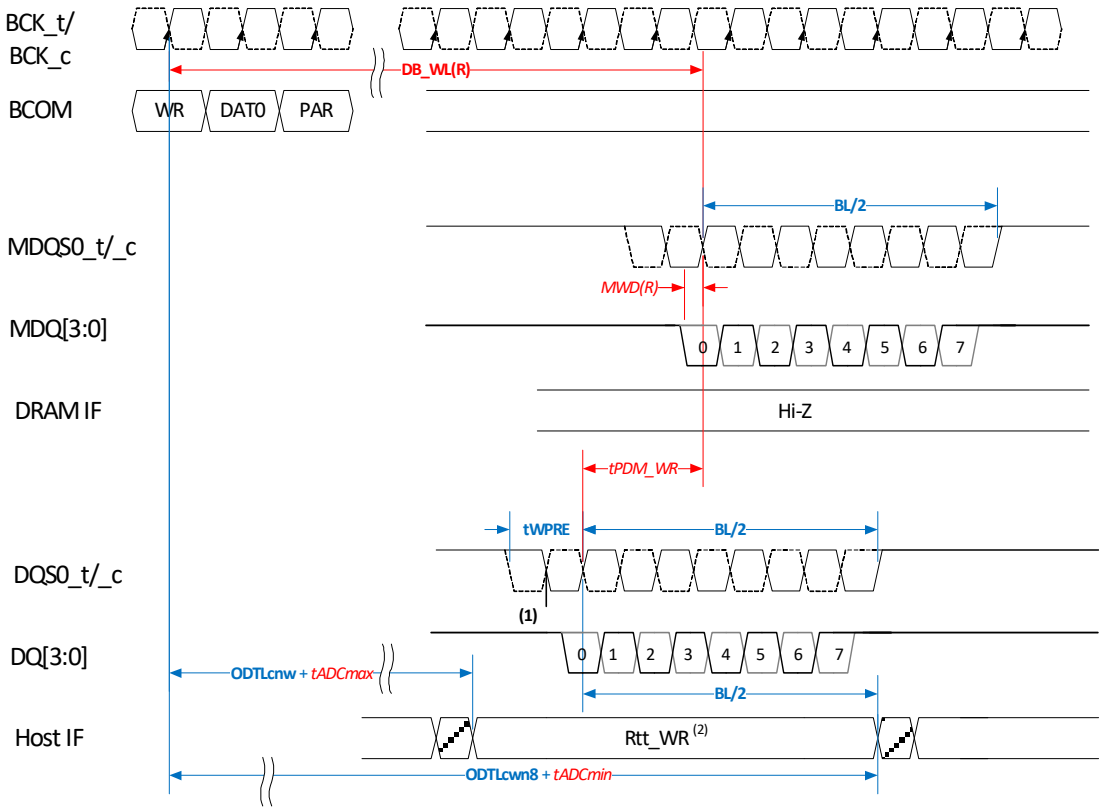
JESD82-32A

(Revision of JESD82-32, November 2016)

AUGUST 2019

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Figure 2 shows the timing sequence for a Write command.



(1) Host Interface Receivers turn-on in the middle of the pre-amble

(2) If Dynamic ODT is enabled in BC01

Figure 2 — WRITE Timing

2.14 Read Commands and MPR Override Reads

Table 5 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 (A[1:0] = '00' or

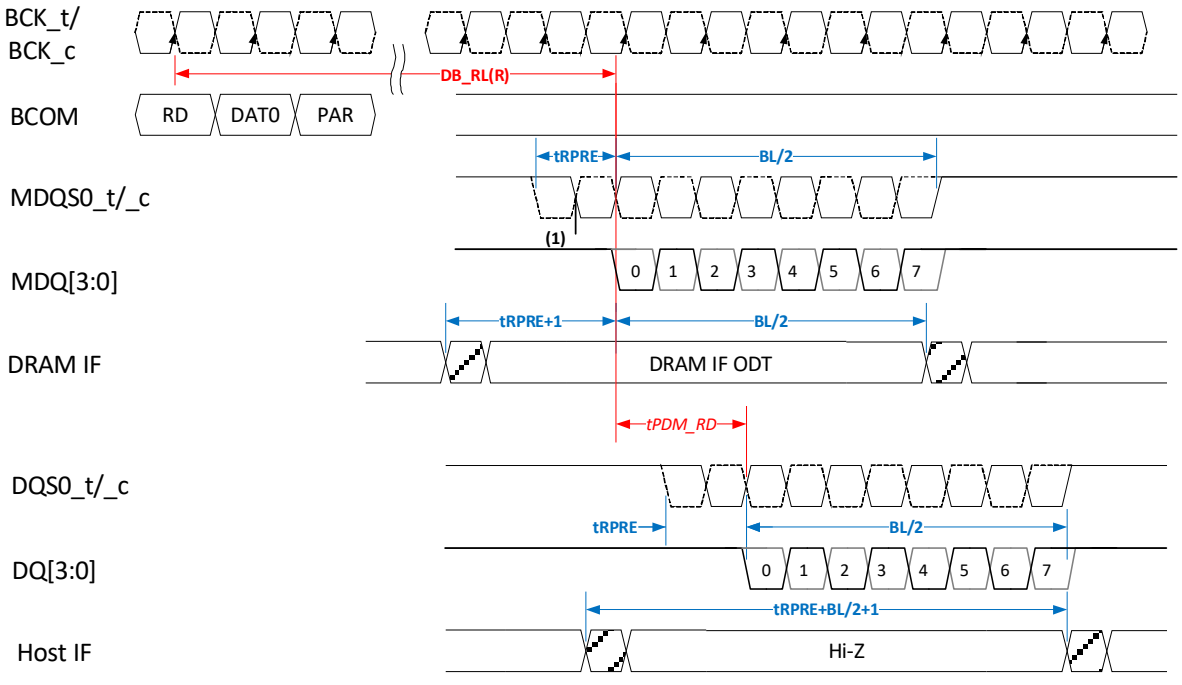
'10').

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

1. BC4 is not supported for MPR override reads

Figure 3 shows the timing sequence for a Read command.



(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

Figure 3 — READ Timing

4.61 Logic Diagram

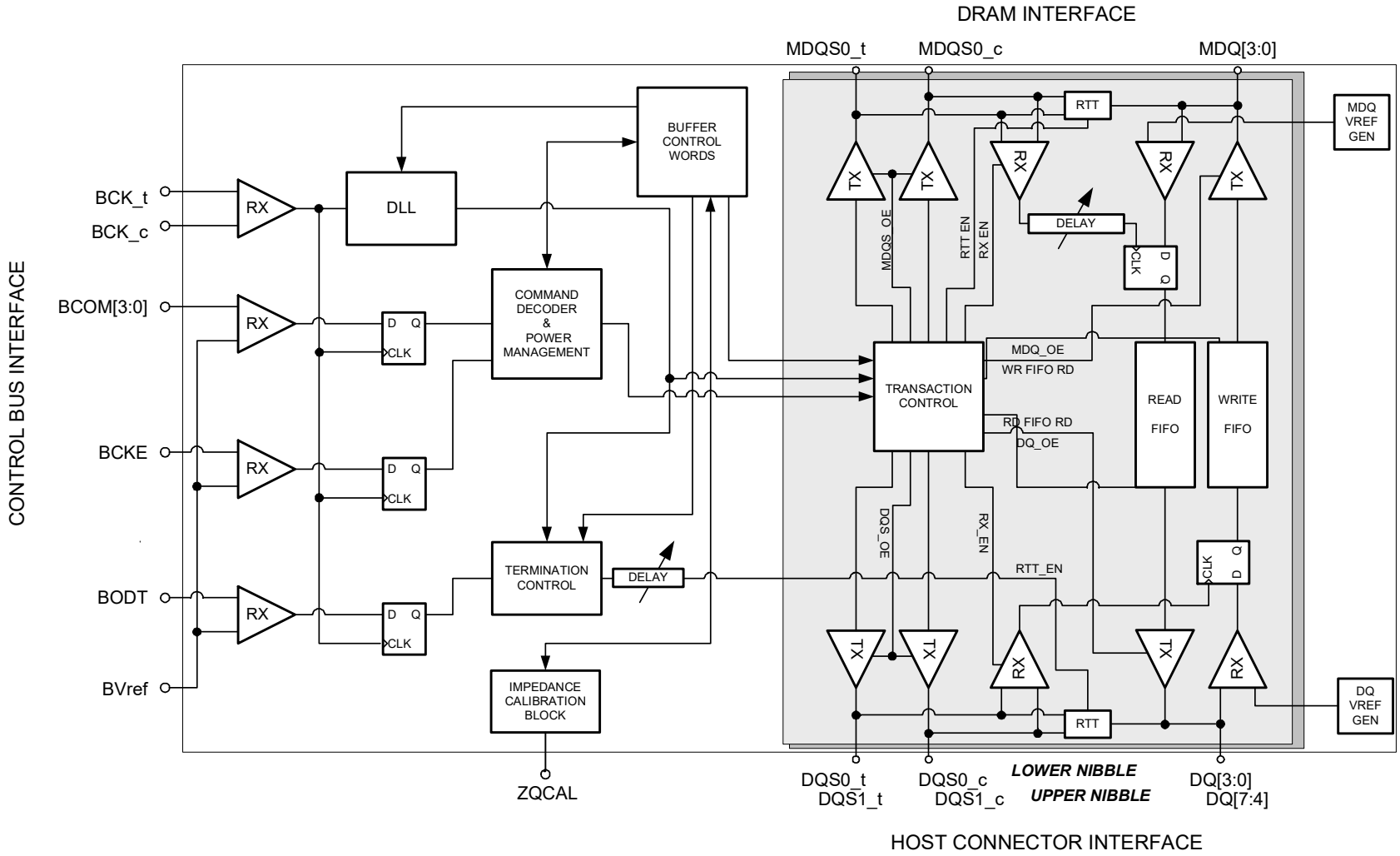


Figure 15 — Logic Diagram

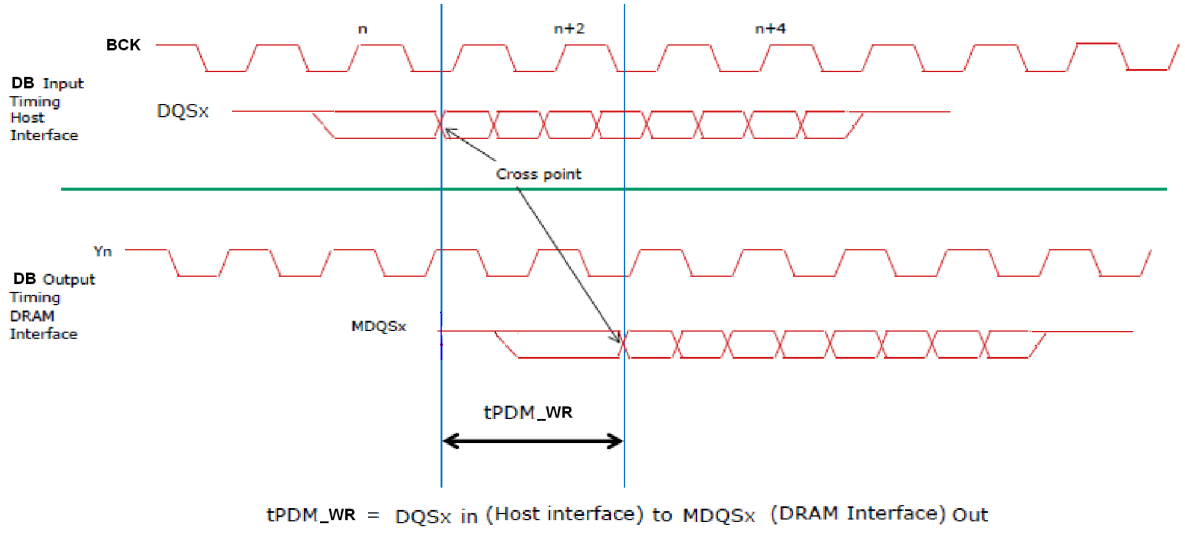


Figure 56 — tPDM_WR Latency Measurement

Table 144 — Output timing requirements in Package Rank Alignment Mode

Symbol	Parameter	Conditions		Min	Max	Unit
$t_{PDM\_RD\_RA}$[1]	MDQS to DQS Propagation Delay	1.2 V Operation[2,3]	Lower Nibble[4]	-	1.67 + tCK/4 + X(R)[5]	ns
			Upper Nibble[4]	-	1.67 + tCK/4 + Y(R)[6]	ns
$t_{PDM\_WR\_RA}$[1]	DQS to MDQS Propagation Delay	1.2 V Operation[2,3]	Lower Nibble[4]	-	1.67 + tCK/4 + Z(R)[7]	ns
			Upper Nibble[4]	-	1.67 + tCK/4 + W(R)[8]	ns

1. Applies when Package Rank Alignment mode is enabled (F0BC1x DA7 = 1). Package Rank Alignment granularity is 1/64*tCK. Upper Nibble and Lower Nibble are not required to be aligned by DDR4DB02.
2. These parameters are only guaranteed after the correct speed range has been programmed in BC0A
3. These timings are only valid with the DA[5:0] bits of the lower and upper nibble read delay and write delay control words (F[3:0]BC4x, F[3:0]BC5x, F[3:0]BC8x and F[3:0]BC9x) at their power on default of 6b'000000 and default slew rate control setting of BC0B DA[3:2] = 00.
4. Maximum temperature and voltage drift must be 170 ps or less for respective nibble.
5. The value of X is rank dependent and it is equal to the difference between MAX(F[3:0]BC2x) and the value of the Fn-BC2x corresponding to each rank. For example, for the earliest rank X = [MAX(F[3:0]BC2x) - MIN(F[3:0]BC2x)], and for the latest rank X = 0. DDR4DB02 supports the largest value of X of 500 ps.
6. The value of Y is rank dependent and it is equal to the difference between MAX(F[3:0]BC3x) and the value of the Fn-BC3x corresponding to each rank. For example, for the earliest rank Y = [MAX(F[3:0]BC3x) - MIN(F[3:0]BC3x)], and for the latest rank Y = 0. DDR4DB02 supports the largest value of Y of 500 ps.
7. The value of Z is rank dependent and it is equal to the difference between MIN(F[3:0]BCAx) and the value of the Fn-BCAx corresponding to each rank. For example, for the latest rank Z = [MAX(F[3:0]BCAx) - MIN(F[3:0]BCAx)], and for the earliest rank Z = 0. DDR4DB02 supports the largest value of Z of 500 ps.
8. The value of W is rank dependent and it is equal to the difference between MIN(F[3:0]BCBx) and the value of the Fn-BCBx corresponding to each rank. For example, for the latest rank W = [MAX(F[3:0]BCBx) - MIN(F[3:0]BCBx)], and for the earliest rank W = 0. DDR4DB02 supports the largest value of W of 500 ps.

Table 146 — WRITE Output Timings

		DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4- 2933		DDR4-3200		Units	Notes
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Data Timing											
tDVB	Data valid before MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
tDVA	Data valid after MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
Data Strobe Timing											
MDQS_t - MDQS_c differential output low time	tMQSL	0.46	-	0.46	-	0.46	-	0.46	-	tCK	1, 3
MDQS_t - MDQS_c differential output high time	tMQSH	0.46	-	0.46	-	0.46	-	0.46	-	tCK	2, 3

Unit UI = tCK(avg).min/2

NOTE 1: tMQSL describes the instantaneous differential output low pulse width on MDQS_t - MDQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 2: tMQSH describes the instantaneous differential output high pulse width on MDQS_t - MDQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

10.6 Package Rank to Package Rank Timing Requirements

Table 147 — DDR4DB02 Operating Spec for Different Package Ranks

		DDR4-1600 to 2400		DDR4-2666/2933		DDR4 -3200			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
TRDRD	Read to Read Command Spacing	tRPRE + BL/2 + 1.8	-	tRPRE + BL/2 + 1.8	-	tRPRE + BL/2 + 1.8	-	tCK(avg)	1, 2, 4, 8
TWRWR	Write to Write Command Spacing	tWPRE + BL/2 + 1.8	-	tWPRE + BL/2 + 1.8	-	tWPRE + BL/2 + 1.8	-	tCK(avg)	1, 2, 5, 8
TRDWR	Read to Write Command Spacing	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7 + (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7+ (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7 + (CL - CWL)	-	tCK(avg)	1, 2, 3, 6, 8
TWRRD	Write to Read Command Spacing	tRPRE/2 + BL/2 + 2.7 - (CL - CWL)	-	tRPRE/2 + BL/2 + 2.7 - (CL - CWL)	-	tRPRE/2 + BL/2 + 2.7- (CL - CWL)	-	tCK(avg)	1, 2, 7, 8

Notes:
1. DDR4DB02 will guarantee the functionality with this minimum command spacing.
2. For operation to same package rank, this restriction does not apply. Host controller follows DRAM JESD79-4 Specification. DDR4DB02 will guarantee the functionality in accordance with DRAM JESD79-4 Specification.
3. This is meant for DDR4DB02 testing on ATE environment purpose to ensure proper buffer functionality. Host controller is likely to require additional separation to avoid the bus contention on Host controller and buffer input interface under normal operation.